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Attorney's Docket No.: 10559-608001/P12892/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Timothy J. Fennell et al. Art Unit: 2825
Serial No.: 10/041,753 Examiner: P. Kik

Filed : January 7, 2002 Assignee : Intel Corporation

Title : REPRESENTING A SIMULATION MODEL USING A HARDWARE

CONFIGURATION DATABASE

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants call attention to the attached Information

Disclosure Statement and documents listed on form PTO-1449.

Copies of the U.S. patents and publications are not being provided per the waiver posted on the PTO website.

Kindly accept this Information Disclosure Statement under Rule 97(c)(2). The rule 17(p) certification fee of \$180 is enclosed.

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

04/16/2004 HBERHE 00000062 10041753

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CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit

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Typed or Printed Name of Person Signing Certificate

Applicant: Timothy J. Fennell et al. Attorney's Docket No.:10559-608001

Serial No.: 10/041,753

Filed : January 7, 2002

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

Please apply any additional charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Dato.

Scott C. Harris Reg. No. 32,030

Attorney for Intel Corporation

Fish & Richardson P.C. USPTO Customer No. 20985 12390 El Camino Real San Diego, CA 92130

Telephone: (858) 678-5070 Facsimile: (858) 678-5099

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Substitute (Modifice)

Form PTO-1449

U.S. Department of Commerce Patent and Trademark Office Attorney's Docket No. 10559-608001

Application No. 10/041,753

Information Disclosure Statement

by Applicant (Use several sheets if necessary) Timothy J. Fennell et al.

Filing Date

Applicant

Group Art Unit

(37 CFR §1.98(b))

January 7, 2002

2825

			U.S. Pate	nt Documents			
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
.,	AA	RE 38,059	04/2003	Yano, et al.			
	AB	4,703,435	10/1987	Darringer, et al.			
	AC	4,970,664	11/1990	Kaiser, et al.			
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	AE	5,267,175	11/1993	Hooper			
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	AK	5,475,605	12/1995	Lin			
	AL	5,493,507	02/1996	Shinde, et al.			
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	AAA	5,841,663	11/1998	Sharma, et al.			

Examiner Signature

Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute (Modified)

Form PTO-1449

U.S. Department of Commerce Patent and Trademark Office

Attorney's Docket No. 10559-608001

Application No. 10/041,753

Information Disclosure Statement by Applicant

(Use several sheets if necessary)

Applicant

Timothy J. Fennell et al.

Filing Date January 7, 2002 Group Art Unit 2825

(37 CFR §1.98(b))

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	ABB	5,892,682	04/1999	Hasley, et al.			
	ACC	5,903,469	05/1999	Но			
	ADD	5,937,190	08/1999	Gregory, et al.			
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	AFF	6,161,211	12/2000	Southgate			
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	AJJ	6,234,658	05/2001	Houldsworth			
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	AVV	6,473,885	10/2002	Wallace			
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	AAAA	6,523,156	02/2003	Cirit			
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Examiner S	Signature
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Date Considered

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Form PTO-1449

U.S. Department of Commerce Patent and Trademark Office Attorney's Docket No. 10559-608001

Application No. 10/041,753

Information Disclosure Statement by Applicant

Timothy J. Fennell et al.

(Use several sheets if necessary)

Filing Date

Applicant

Group Art Unit

(37 CFR §1.98(b))

January 7, 2002

2825

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Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate	
	ACCC	6,546,528	04/2003	Sasaki, et al.				
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	AEEE	6,591,407	07/2003	Kaufman, et al.				
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	Alii	0 404 482	12/1990	EPO				
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	AKKK	0 720 233	07/1996	EPO				
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	AQQQ	08-314892	11/1996	Japan				
	ARRR	2001-068994	03/2001	Japan				
	ASSS	WO 98/37475	08/1998	WIPO				
	ATTT	WO 00/65492	11/2000	WIPO				

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	AUUU	Kutzschebauch, "Efficient logic optimization using regularity extraction", Proceedings of 2000 International Conference on Computer Design, September 17, 2000, pp. 487-493.					
	AVVV	Maxfield, C., "Digital Logic Simulation: Event-Driven, Cycle-Based, and Home-Brewed", Electrical Design News, 41(14):129-136 (1996).					
	AWWW	NB84035598, "Binary Relational Schema to Model Structured LSI Design", IBM Technical Disclosure Bulletin, Vol. 26, No. 10B, March 1984, pp. 5598-5601.					

Examiner Signature

Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Form PTO-1449 (Modified)

U.S. Department of Commerce Patent and Trademark Office

Attorney's Docket No. 10559-608001

Application No. 10/041,753

Information Disclosure Statement by Applicant (Use several sheets if necessary)

Timothy J. Fennell et al.

Filing Date

Applicant

Group Art Unit

(37 CFR §1.98(b))

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2825

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	AXXX	NN7807629, "Functional Oriented Symbolic Macromodeling Algorithm", IBM Technical						
	AAAA	Disclosure Bulletin, Vol. 21, No. 2, July 1978, pp. 629-631.						
	AYYY	NN8006341, "Macro Physical-To-Logical Checking LSI Chip Design", IBM Technical Disclosure						
	Alli	Bulletin, Vol. 23, No. 1, June 1980, pp. 341-345.						
	AZZZ	NN9407481, "Functional Modeling using object Collaboration Diagram", IBM Technical Disclosure						
	ALLL	Bulletin, Vol. 37, No. 7, July 1994, pp. 481-486.						
		Parlakbilek, et al., "A Multiple-Strength Multiple-Delay Compiled-Code Logic Simulator", IEEE						
	AAAAA	Transactions on Computer-Aided Design of Integrated Circuits and Systems, 12(12):1937-1946						
		(1993).						
	ABBBB	Su, Stephen, "An Interactive Design Automation System", Proceedings of the 10th Design						
		Automation Workshop on Design Automation, pp. 253-261, June 1973						

Examiner Signature

Date Considered